CLAIMS

What is claimed is:

Sub C1

1. A computer implemented method of generating an order of loading data into a programmable device comprising the steps of:

a) identifying a plurality of memory cells in a hierarchical schematic representation of said programmable device;

b) automatically determining a plurality of addresses corresponding to said plurality of memory cells;

c) automatically determining a plurality of logical names for said plurality of memory cells; and

d) based on an order in which said plurality of addresses are to be loaded into said programmable device, automatically storing said plurality of logical names for said plurality of memory cells within a data structure within computer readable memory.

2. The method of Claim 1 wherein step a) comprises the step of:

a1) identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy.

3. The method of Claim 1 wherein step b) comprises the steps of:

b1) determining a wordline associated with one memory cell of said plurality of memory cells; and

b2) determining a bitline associated with said one memory cell of said plurality of memory cells.

4. The method of Claim 1 further comprising the step of:

e) repeating said steps a) through d) for each configuration block of said programmable device.

5. The method of Claim 1 further comprising the step of:

e) determining whether there is a configuration bit at said address in said configuration block.

6. The method of Claim 5 further comprising the step of:

f) placing a spacer in said data structure of said plurality of logical names in said step d) responsive to a determination of step e) that there was no configuration bit at said address in said configuration block.

7. The method of Claim 1 wherein said programmable device is a complex programmable logic device (CPLD).

8. A computer implemented method of generating an order of loading data into a programmable logic device comprising the steps of:

a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses;

b) accessing a data structure specifying an order in which said plurality of addresses are to be loaded into said programmable logic device;

c) ordering said plurality of logical names from step a) based on the order specified in said data structure in step b); and

d) storing said ordered plurality of logical names from step c) in a data structure within computer readable memory.

9. The method of Claim 8 further comprising the step of:

e) storing a placeholder in said data structure of said plurality of logical names from step d).

10. The method of Claim 8 further comprising the step of:

e) determining whether there is a configuration bit at one address of said plurality of addresses.

11. The method of Claim 8 wherein step a) further comprises the steps of:

a1) identifying a plurality of memory cells in a hierarchical schematic representation of said programmable device;

a2) identifying said plurality of addresses corresponding to said plurality of memory cells; and

a3) determining said plurality of logical names for said plurality of memory cells.

12. The method of Claim 11 wherein said plurality of memory cells are configuration bits.

13. The method of Claim 11 wherein step a) comprises the step of:

a) identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy.

14. A system comprising a processor coupled to a bus and memory coupled to said bus wherein said memory contains processor instructions for implementing a method of generating an order of loading data into a programmable logic device, said method comprising the steps of:

a) identifying a plurality of memory cells in a hierarchical schematic representation of said programmable device;

b) automatically determining a plurality of addresses corresponding to said plurality of memory cells;

c) automatically determining a plurality of logical names for said plurality of memory cells; and

d) based on an order in which said plurality of addresses are to be loaded into said programmable logic device, automatically storing said plurality of logical names for said plurality of memory cells within a data structure within computer readable memory.

15. The method of Claim 14 wherein step a) comprises the step of:

a1) identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy.

16. The method of Claim 14 wherein step b) comprises the steps of:

b1) determining a wordline associated with one memory cell of said plurality of memory cells; and

b2) determining a bitline associated with said one memory cell of said plurality of memory cells.

Sub A5

17. The method of Claim 14 further comprising the step of:

e) determining whether there is a configuration bit at said address in said configuration block.

18. The method of Claim 17 further comprising the step of:

f) placing a spacer in said data structure of said plurality of logical names in said step d) responsive to a determination of step e) that there was no configuration bit at said address in said configuration block.

19. The method of Claim 14 wherein said programmable device is a complex programmable logic device (CPLD).

20. The method of Claim 14 further comprising the step of:

e) repeating said steps a) through d) for each configuration block of said programmable logic device.

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